CTL CENTER FOR TECHNOLOGY LICENSING AT CORNELL UNIVERSITY

THE TECHNOLOGY

High-performance, highly pipelined asynchronous FPGAs employ a very fine-grain pipelined logic block and routing interconnect architecture. These FPGAs, which do not use a clock to sequence computations, automatically "self-pipeline" their logic without the designer needing to be explicitly aware of all pipelining details. The FPGAs include arrays of logic blocks or cells that include function units, conditional units and other elements, each of which is constructed using basic asynchronous pipeline stages, such as a weak condition half buffer and a precharge half buffer.

Patent	US 7,157,934
Issued	Jan 2, 2007
Inventors	Rajit Manohar & John Teifel
Licensee	Achronix Semiconductor Corporation

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THE PRODUCT

Speedster®

Speedster® Field Programmable Gate Arrays (FPGAs) are the world's fastest programmable logic devices. Speedster® is fully reprogrammable, yet still capable of operating at up to 1.5 GHz system performance, which represents a three-fold increase in performance over existing FPGAs. Speedster® is suitable for a wide range of telecommunications, networking, video, digital signal processing, high-performance computing, imaging, industrial and military applications.

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